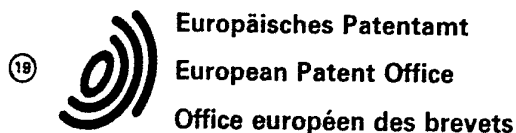


EXHIBIT FP1 TO EXHIBIT H



11 Publication number:

0 154 051
A1

12

EUROPEAN PATENT APPLICATION

21 Application number: 84201831.9

51 Int. Cl.⁴: **G 06 F 9/38**
G 06 F 7/48

22 Date of filing: 11.12.84

30 Priority: 27.12.83 NL 8304442

43 Date of publication of application:
11.09.85 Bulletin 85/37

84 Designated Contracting States:
DE FR GB IT

71 Applicant: **N.V. Philips' Gloeilampenfabrieken**
Groenewoudseweg 1
NL-5621 BA Eindhoven(NL)

72 Inventor: **Van Wijk, Franciscus Johannes Antonius**
c/o INT. OCTROOIBUREAU B.V. Prof. Holstlaan 6
NL-5656 AA Eindhoven(NL)

72 Inventor: **Van Meerbergen, Jozef Louis**
c/o INT. OCTROOIBUREAU B.V. Prof. Holstlaan 6
NL-5656 AA Eindhoven(NL)

72 Inventor: **Welten, Fransiscus Peter Johannes Mathijs**
c/o INT. OCTROOIBUREAU B.V. Prof. Holstlaan 6
NL-5656 AA Eindhoven(NL)

72 Inventor: **Sluijter, Robert Johannes**
c/o INT. OCTROOIBUREAU B.V. Prof. Holstlaan 6
NL-5656 AA Eindhoven(NL)

74 Representative: **Strijland, Wilfred et al,**
INTERNATIONAAL OCTROOIBUREAU B.V. Prof.
Holstlaan 6
NL-5656 AA Eindhoven(NL)

54 Integrated and programmable processor for word-wise digital signal processing.

57 A description is given of an integrated and programmable processor for word-wise digital signal processing. The processor comprises a multiplier element, an arithmetic and a logic unit (122), a data memory and a connection for a control memory which may be integrated on-chip. The elements are interconnected by means of a double bus (20, 22) on which addresses as well as data may be transported by means of suitable selectors. Consequently, a pipeline operation can also take place within one instruction cycle.

EP 0 154 051 A1

./...

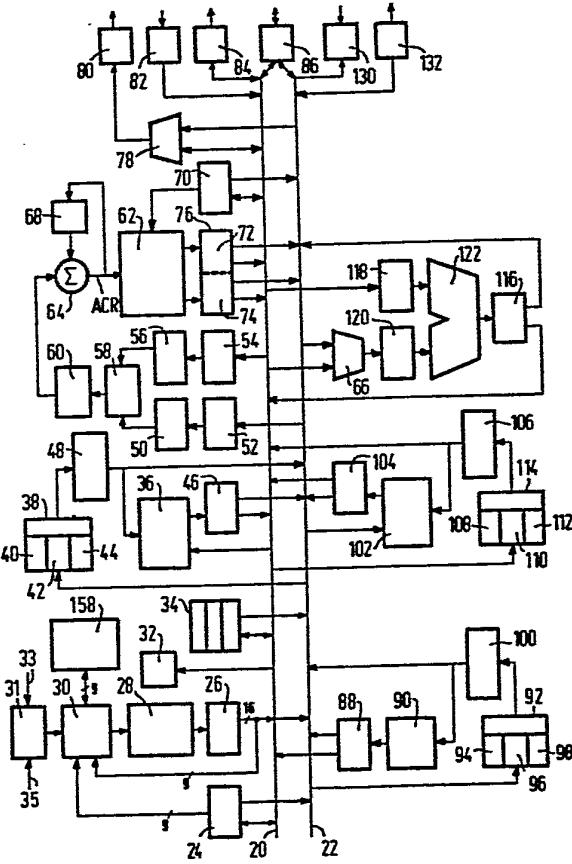


FIG.1

PHN 10 886

1

0154051

"Integrated and programmable processor for word-wise digital signal processing".

Background of the invention:

The invention relates to an integrated and programmable processor for word-wise digital signal processing, comprising:

- 5 a. a multiplier element which comprises a first input and a second input for receiving two operands for multiplication and a first output for presenting a product;
- b. an arithmetic and logic unit which comprises a third
10 input and a fourth input for receiving two further operands, a second output for presenting a result operand, and first accumulator means which are connected between the second output and the third input;
- c. a first read-write memory for the storage of data;
- 15 d. connection means for connecting a control memory for the storage of control information for the other components;
- e. communication means, including bus connection means, for
20 connecting said components to one another and to the environment.

A data processor of this kind is known from European Patent Application 0086307-A2 assigned to Texas Instruments Corporation. The known device is an integrated micro-computer in which a program bus and a data bus are provided
25 on the chip; the exchange of program information with the environment is also possible. Furthermore, the output of the multiplier element is directly connected to one of the inputs of the arithmetic and logic unit. It has been found that the flexibility of such a processor cannot be
30 high because of inter alia such a very direct coupling. It has also been found that the presence of only one data bus also reduces the flexibility of the processor. "Bus" is to be understood to mean herein an interconnection between

PHN 10 886

2

0154051
31-8-1984

at least three stations, with at least two possible information sources and at least two possible information destinations.

Summary of the invention:

5 It is an object of the invention to provide an integrated data processor which offers a wide variety of uses and which allows high-speed signal processing. Generally, signal processing reads operations which are executed in "real time", so that notably each operation must be
10 completed within a fixed time interval. Such signal processing operations are often executed as vector operations, which means the formation of a sum of a series of products in which successive signal values form one of the factors each time. Typically the same operations are constantly re-
15 peated on successive signal words of a block or series of signal words. However, often other types of operations such as are usually executed in an arithmetic and logic unit (ALU) are also necessary, for example bit-wise formation of an OR-function, rotation or shifting.

20 The object is achieved in that the invention is characterized in that
f. said first input is connected to a separate first bus, said second input and fourth input being connected to a separate second bus of said bus connection means;
25 g. said third input can be coupled to the first bus;
h. said first accumulator means comprise a third output with a first selector for forming a selectable connection to said first and second bus;
i. said first output comprises a second selector for forming
30 a selectable connection to said first and second bus;
j. said first read/write memory comprises an address input and a data input which are connected to said first and second bus, and a fourth output with a third selector in order to form a selectable connection to said first
35 and second bus.

This structure is based on the recognition of the fact that a firm coupling between multiplier element and arithmetic and logic unit is usually open to objection for the exe-

PHN 10 886

3

31-8-1984 **0154051**

cution of a mixture of vector operations and other operations in one program. On the one hand, many vector operations only require the multiplier element. Interjection of the arithmetic and logic unit would then cause a delay. For the execution of many other operations, only the arithmetic and logic unit is required. In that case the interjection of the multiplier element would cause a delay. Therefore, it is better to keep the two operations separate, so that the arithmetic and logic unit and the multiplier element can be optimized as regards function spectrum as well as processing speed. The two-bus structure connected to the relevant inputs and outputs in the manner specified increases the flexibility and the processing speed further. For example, for the development of a given program use can now be made of an external control memory which is constructed, for example, as an electrically variable memory (NVRAM, RAM, PROM, EPROM or EEPROM). For mass production, however, it will usually be integrated as a programmable read-only memory (E^2 PROM, EPROM) or read-only memory (ROM). The latter memories are cheaper; for example, a read-only memory occupies only very little space on the chip.

Preferably, said first read/write memory comprises a first memory module whose address input is connected to the first bus and whose data input is connected to the second bus, and a second memory module whose address input is connected to the second bus and whose data input is connected to the first bus, the third selector comprising for each memory module a corresponding selection module which is connected to each of the two buses, the connection for the control memory comprising an instruction register for storing control information for the control of further components, said instruction register also having a data output connected to said bus connection means. Data can thus always be routed in a variety of ways before and after the relevant operations.

Preferably, each of said first and second memory modules comprises its own address calculation unit. A higher flexibility can thus be achieved.

Preferably, said first output comprises retro-

PHN 10 886

4

30.8.1984
0154051

coupled second accumulator means, including accumulator adder means, whereto there is connected a shift unit for performing selectable shift and reformatting operations on data to be applied to the bus connection means. Thus, the multiplier element allows for a large number of different operations to be performed without requiring the bus connection means; the latter may then be operative for a preceding or the next processing operation.

Preferably, said first accumulator means comprise a second read/write memory which is capable of storing several operands and which comprises triple addressing means in order to allow for the simultaneous execution of a write operation from the arithmetic and logic unit as well as two independent read operations to and from the first and the second bus, respectively. Thus, a local and hence freely accessible processing memory is available to the ALU unit, so that the execution of a wide range of operations is facilitated.

Preferably, there are provided further connection means for a further data memory which is constructed as a read-only memory and which comprises an address connection to said bus connection means and a selectable data connection to said first and second bus. Such a read-only (data) memory can be advantageously used notably for the storage of coefficient information for said vector operations; as regards the desirability of integration or not, the same holds good as for the control memory already described.

Preferably, said third input comprises selector means for forming a selectable connection to said first and second bus. The arithmetic and logic unit is capable of performing operations on one or on two operands. Thanks to the latter facility, it is now possible to present this single operand each time on the same input of the arithmetic and logic unit, so that the configuration of the latter unit may be simpler.

Preferably, there are provided timing means for

PHN 10 886

5

0154051
30.8.1984

controlling a first instruction cycle which comprises the following coincident operations:

- address calculation for a data memory, including associated memory access, in order to make an operand for the bus connection means available during the next instruction cycle;
- a data transport via at least one bus of the bus connection means; and
- a data processing operation in at least either the arithmetic and logic unit or the multiplier element on an operand transported via the bus connection means during said instruction cycle in order to form a result operand during this instruction cycle which is made available for transport via the bus connection means during the next or a later instruction cycle. A given degree of parallelism can thus be achieved within one instruction cycle.

Preferably, there is provided a cycle selector which comprises a first state and a second state in order to control in the first state said first instruction cycle and in the second state a second instruction cycle having a length which amounts to half the length of the first instruction cycle, said second instruction cycle comprising the following coincident operations:

- address calculation for a data memory for the formation of an address for the next instruction cycle;
- memory access in a data memory by means of an address calculated during the directly preceding instruction cycle in order to make an operand available for the bus connection means in the next instruction cycle;
- a data transport via at least one bus of the bus connection means;
- a data processing operation in at least one of the two elements arithmetic and logic unit and multiplier element on at least one operand transported via the bus connection means during said instruction cycle or during a previous instruction cycle in order to form a result operand during the interval of the same instruction cycle puls the next

PHN 10 886

6

309-54051

instruction cycle in order to make this operand available for transport via the bus connection means during the second next instruction cycle or during a later instruction cycle, for which purpose output registers are connected to the multiplier element, and to the first read-write memory, said output registers being transparently activatable in said first state of the cycle selector, there being provided input registers for the arithmetic and logic unit and the multiplier element which are transparently activatable in both states of the cycle selector. By the interjection of the additional registers, uncoupling takes place so that the signals on the input thereof (result of an operation) are uncoupled from the signals on the output of these registers (result of a preceding operation).

Due to this uncoupling, a higher processing speed can be achieved without a faster technology being required or a higher clock pulse frequency being used. The processing speed is also increased by extension of the parallel pipelining principle as will be explained in detail hereinafter. It is a minor drawback, however, that programming is now slightly more complex because each instruction word must contain elements of operations whose further execution is controlled only by later instruction words.

Some further attractive details are specified in the sub-claims.

Brief description of the figures:

The invention will be described in detail hereinafter with reference to the drawings. First a description will be given of a general block diagram of a preferred embodiment, followed by a description of some detailed diagrams and operations,

Fig. 1 shows a general block diagram of a data processor in accordance with the invention;

Fig. 2 illustrates the four types of instructions which can be executed;

Fig. 3 shows a time diagram for the execution of a standard instruction in a normal cycle;

PHN 10 886

7

0154051
30.8.1984

Fig. 4 shows a time diagram for the execution of a standard instruction in an accelerated cycle;

Fig. 5 shows a block diagram of an address calculation unit;

5 Fig. 6 illustrates the set of instructions of an address calculation unit;

Fig. 7 illustrates the shift/reformatting unit;

Fig. 7a shows the functions to be realized therein;

10 Fig. 8 illustrates the arithmetic and logic unit;

Fig. 9 illustrates the local processing memory;

Fig. 10 illustrates the serial data output;

Fig. 11 illustrates the serial data input;

15 Fig. 11a illustrates the parallel data input/output;

Fig. 12 illustrates the program status register;

Figs. 13a, b, c, d illustrate a part of the instruction code;

Figs. 14, 14a illustrate the multiplier element;

20 Fig. 1 shows a general block diagram of the data processor in accordance with the invention. The internal connection is realized by a first 16-bit data bus 22 and a second 16-bit data bus 20. The circuit comprises a number of registers, some of which are directly connected to one
25 of the two buses, that is to say elements 24, 26, 34, 46, 48, 50, 56 (the latter two elements via a selection element). 70, 72, 74, 88, 100, 104, 106, 118, 120, 124, 126. Element 30 is a program counter which addresses a program memory 28 having a capacity of 512 words of 40
30 bits which can be loaded into the output register 26. The execution of these instructions will be described in detail hereinafter: most bits control further functions in the remainder of the circuit via connections/decoders which have been omitted for the sake of simplicity. A 16-bit portion
35 can be applied in parallel to both data buses for one type of instruction. Program counter 13 can be loaded either with 9 bits from the instruction register 26 or with an

PHN 10 886

8

0154051
30.8.1984

address from an 8-word stack register 158. The register 24 acts as an interrupt address register and is asymmetrically connected between the two buses (i.e. in the same manner as elements 34, 70, 78 to be described hereinafter: unidirectionally to the bus 22, bidirectionally to the bus 20). This restriction is not essential; for a long instruction word, the number of different functions to be controlled would be larger so that a more universal connection pattern would be feasible. If desired, the memory 28 is not integrated but constructed as a "separate" memory in order to facilitate the programming; in that case forty additional pins are added to the integrated circuit in order to supply the instruction register 26 with information. Preferably, at least 9 of these forty pins are bidirectionally operative for the supply of an address to the external memory. In a specific embodiment (not shown), the latter number is chosen to be 16, so that the width equals that of the data buses. These forty connection pins operate in time multiplex: alternately address and data.

Element 90 is a data memory which is constructed as a read-only memory for 512 words of 16 bits in the present embodiment. If desired, the memory 90 is not integrated but constructed as a "separate" memory in order to facilitate programming; in that case sixteen additional pins are included in the integrated circuit for the supply of information to element 88. Nine of these 16 pins are bidirectionally operative for the supply of an address to the external memory. They are again operative in time multiplex. Furthermore, elements 36, 102 are data memory modules, elements 38, 92, 114 are address calculation units, and elements 66, 78 are selectors for the two buses. Registers 48, 100, 106 are associated with the address calculation means which will be described in detail with reference to Fig. 5. Furthermore, as is apparent some registers (for example, 88, 104 46, 72, 74, 34) have selective connections to the two buses. Registers 50, 56

0154051

PHN 10 886

9

30.8.1934

operate as registers which are or are not transparent
 Element 58 is a 16 x16 bit multiplier element with an
 associated control register 70. Element 64 is a 40-bit
 accumulator adder. Element 68 is a 40-bit accumulator
 5 register. Element 78 is a bidirectional selector. Element
 122 is an arithmetic and logic unit. Element 116 is a
 memory comprising 3 connections (ports) which is used as
 a set of scratchpad or processing memories. Furthermore,
 element 128 is an input/output control element and elements
 10 80, 82, 84, 86, 130, 132 are input/output units for
 communication with the environment.

The registers have the following functions:

| | | |
|-----------|---|--|
| 24 | : | instantaneous address register for RAM 36 (ARA) |
| 15 46 | : | data register connected to the output of RAM 36 (DRA) |
| 106 | : | instantaneous address for RAM 102 (ARB) |
| 104 | : | data register connected to the output of RAM 102 (DRB) |
| 20 50, 56 | : | two registers, transparent or not, which are connected to the inputs of the multiplier element. |
| 25 | | During a machine cycle, either the signal arriving on the input appears on the output of the relevant register (transparent) or the signal present in the register itself appears thereon (not transparent). At the end of such a cycle, the signal then present on the input of the register (MXL, MYL) |
| 30 | | is always stored in the register. |
| 60 | : | product register (PR) |
| 68 | : | accumulator register (ACR) |
| 72/74 | : | register sections for the most-significant and the least significant product portion |
| 35 | | (MSP, LSP) |
| 70 | : | register for the control of the shift element 62 as regards the shifting and the format selection and possibly bit reversal (BSR) |

PHN 10 886

10

0154051
1-9-1984

- 118, 120 : two registers which operate transparently or not and which are connected to the input of the ALU 122 (AXL, AYL)
- 116 : fifteen scratchpad registers (R0 ... R14), also representing an accumulator function; physically, this element acts as a memory having three independent access facilities with as many independent addresses and two data outputs and one data input
- 40, 94, 108 : basic address registers (AA, RA, BA)
- 42, 96, 110 : shift address registers (AS, RS, BS)
- 44, 98, 112 : address masking registers (AM, RM, BM)
- 84, 130 : serial output registers for the two buses (SOX, SOY)
- 82, 132 : serial input registers for the two buses (SIX, SIY)
- 86 : multiplexed parallel input/output register (PO, PI)
- 80 : additional parallel output register (ADO).

Functional description:

Synchronized by a clock which is not separately shown, the data processor is capable of executing up to 10 million instructions per second. This is achieved in that several instructions can be executed in parallel by way of a pipeline organization. The two parallel operating data buses are operative to accelerate the transport. Communication with the environment is provided by powerful I/O interface units for serial as well as parallel communication. There are provided three data memories, that is to say two read-write memories and one read-only memory, each comprising its own address calculation unit. The arithmetic and logic unit 122 has a set of instructions yet to be described. The multiplier element 58 is combined with a 40-bit accumulator 64/68 and a general purpose shift unit 62.

The inventors have recognized the fact that in some cases it will be advantageous for one or both buses to have a larger bit width, for example 24 bits. In some

PHN 10 886

10a

~~10154051~~
0154051

cases it will not be necessary to connect all elements to all 24 bit lines. Depending on the circumstances, for given elements this may be restricted to 16 or even 12 bits. Furthermore, in order to save components it will
5 in some cases be permissible to combine the addressing unit of a (read-only) memory and a data memory.
Summary of the instruction set.

Fig. 2 illustrates the four types of instructions which can be executed. The first two bits indicate the type

10

15

20

25

30

35

PHN 10 886

11

0154051
~~31181994~~

The first arithmetic instruction controls in parallel an operation in the arithmetic and logic unit, a bus transport via at the most two buses, and at the most three address calculations. The second arithmetic instruction is the counterpart of the first instruction and controls an operation in the multiplier element. The field AIIS/OPS or MINS controls the operation, SX/DX or SY/DY controls the source elements or destination elements on the two buses, respectively, RFILE acts as an address for the local memory 116, and ACUA, ACUB, ACUR are operative or the control of the address processing elements.

In the third instruction, the branch instruction, the bits 3 to 18 contain a destination address for the branch. BR indicates the type of brach instruction and COND the condition. The bit positions 2 and 27 to 39 are void. Alternatively, also this instruction may contain the ACU fields recited hereabove, are now also included in these fields in this particular operating mode.

In the fourth instruction, direct loading, the field DATA indicates the data to be transported on the bus, and the other fields are operative as in the arithmetic instructions. The details of these instructions will be described herein-after.

Under standard conditions each one-word instruction can be executed in 200 ns. With a given program control this can be reduced to 100 ns. This is achieved by elaboration of the pipeline priciple as will be described in detail herein-after. In this respect Fig. 3 shows a time diagram of a standard 200 ns instruction cycle. The time diagram of an accelerated instruction cycle as shown in Fig. 4 will be described herinafter. Line 200 in Fig. 3 contains the sequence of instruction time intervals having a length of 200 ns. Crossing lines indicate the connections to preceding/ subsequent intervals. Line 202 shows the operations for the fetching of operands. Block 1 offers time space for any calculation of a read address. Due to the organization of the separate memories 36, 102 and 90, this can be performed in an arbitrary combination of these three memories (possibly even in all three memories simultaneously).

PHN 10 886

12

~~0154051~~

Furthermore, the relevant memory is read. In as far as a memory serves to supply an operand, in interval/block 2 the information on this line of the relevant location of this memory is valid on the output. On line 204 the processing
 5 of the data is symbolized. Block 1 offers time space for the transport of the data on one of the two (or both) transport buses and, whenever applicable, for the actual processing in the multiplier element and/or the arithmetic and logic unit. In given circumstances, however, such an operation will
 10 not be activated, for example when only a register to register transfer is performed. During block 2 on this line, any data thus obtained is valid on the output of the relevant processing element. Line 204 shows the further output of the data thus formed. Block 1 thereof offers space for the calculation
 15 of an address in one of the two (or both) read-write memories. Block 2 offers time space for the transport via one or both buses 20, 22, possibly to a read-write memory; to this end, an address is then calculated in block 1 of line 206. Thus, between the beginning and the end of an instruction there
 20 are three blocks of 200 ns. During the second one of these blocks, however, an address calculation can already be performed for the next instruction. During the third block of this cycle, the processing (multiplier element cum accumulator and/or arithmetic and logic unit) can already
 25 be performed for the next instruction. During the execution of an instruction in the described manner, the bit FQR in the program status register PST in the element 34 has the value "0". A second, faster operating mode will be described later.

30 Detailed description of the sub-systems:

1) Program memory 28

This memory is addressed by the program counter 30. This counter has the incrementation function (address +1) and the "constant" function (address not modified). Furthermore,
 35 the following functions can be performed:

- a CALL instruction
- a JUMP instruction
- a RETURN instruction.

PHN 10 886

13

~~0154051~~

The program counter 30 is controlled by the control unit 31 which comprises a reset input 33 and an interrupt input 35. The state is co-controlled by :

- register 32 which indicates an instruction repeat:
 - 5 - register bank 34 which contains condition information in register PST for said instruction categories, and also instruction cycle information (FQR) and information concerning the permissibility of interrupts.
- These registers 32, 34 can be loaded (34 may also serve
10 as a data source) from the bus 20; therefore, they are asymmetrically connected to both buses.

The actual program counter 30 (9 bits) fulfills the following functions:

- in response to the fetching of each instruction from the
15 memory 28 to the instruction register 26, the program counter is incremented. Upon execution of one of the subsequent, conventional instructions, the value of the address field is transferred as a new address to the program counter:
- 20 jump instructions (if feasible)
 - call instructions (if feasible).

For the latter (call) instructions, the content of the program counter is written in the upper register of the stack (8) of registers 158 after incrementation by +1.

- 25 When a return instruction is executed, the content of the uppermost register of the stack is transferred to the program counter. The interrupt address from the register 24 is transferred to the program counter when the interrupt bit ($\overline{\text{INT}}$) on input 35 gets value 0 while the interrupt is
- 30 permitted in that the relevant enable bit IE of the register PST has the value "1" and the value of the program counter content incremented by 1 is written on the uppermost stack register.

- 35 The register stack comprises 8 registers of 9 bits in a last-in-first-out organization, so that a nested structure of at the most 8 levels is permissible among the subroutines/interruptions.

2) The data memory modules 36, 102, 90.

PHN 10 886

14

31-8-1984 **0154051**

The read-only memory 90 has a capacity of 512 words of 16 bits each; the other two modules each have a capacity of 256 words of 16 bits each. The address lengths amount to 9 bits and 8 bits, respectively. The data inputs of the memories 36, 102 are asymmetrically connected to the buses 20, 22. Via selectors, the data outputs are symmetrically connected to the buses, the data being transported via either one or both buses as desired. When the described slow instruction cycle is activated, the output registers 46, 88, 104 are continuously transparent.

3) Address calculation units.

The address calculation units 38, 92, 41 of the present embodiment are identical, except for their word length of 8 bits and 9 bits, respectively. The address calculation can be coexistent with two arithmetic/move instructions and the load immediate instruction; the address calculations can thus be equickly executed.

The block diagram of such an address calculation unit shown in Fig. 5 comprises the bus 208 (one of the two buses 20, 22 in Fig. 1) and also all elements up to the connection 232 for the actual memory matrix cum address decoder. At the input side there are provided three registers

210 : for the address mask;
 212 : for the actual address where the calculation starts;
 213 : for the shift (offset).

The content of these three registers can be retained at the beginning of an interrupt operation for later use during a further operation. Element 214 is an arithmetic and logic unit having a limited bit width and a limited range of operations (with respect to element 122 in Fig. 1). The element 206 is a masking element in which the calculation result of the element 214 can be bit-wise conducted or blocked by the content of the masking register 210. The output of the masking element 216 is connected to the A register 212. Furthermore, in the reversing element

0154051

31.8.1984

PHN 10 886

15

218 the bit sequence can be reversed. The result from the element 218 can be stored in the actual address register 230. The latter register can also be filled directly by data on (a part of) the lines of the 16-bit bus. The masking in the
 5 element 216 can be used for cyclically passing through the addressees according to a given modulo value; the reversal of the bit sequence is used in given versions of Fourier transform calculations. When a masked value ("0") is received in the modulo register 210, the relevant bit position in the
 10 register 230 remains unmodified. However, when a value ("1") is received in the modulo register 210, the relevant bit position 230 is updated with a new value. In given circumstances the relevant position may have been the subject of a reversing operation. The control of the register 230 in this
 15 respect is denoted by a dotted connection. Actually there is provided a control unit which controls the operations described hereinafter.

In this respect Fig. 6 shows the set of instructions of the address calculation units. They are controlled
 20 by relevant fields in the instruction word: C31-33 for the element 38, C34-36 for the element 114, C37-39 for the element 92 (this word is present in the already described register 26). Fig. 6 is divided into two halves; the upper half is applicable when the relevant unit has not been
 25 selected as the data destination under the control of the fields DX and/or DY of the micro-instruction word to be described hereinafter. In the opposite case the lower half of the Figure is applicable. The first column shows the mnemonics, the second column the bit pattern, the third to
 30 sixth columns the new content for each of the four registers 230, 212, 213, 210 for which "BUS" means that the register is filled with new data from the bus. (A+1) mM means that the address (A+1) is masked by the content of the masking register M; correspondingly, for example, for A-1, A+S and
 35 so on. "BR" means that the bit sequence is reversed. The instruction LALL means that the content of the bus (in as far as supplied) is bit-wise

PHN 10 886

16

3008-5981
~~01-54051~~

inverted. During the loading of the relevant address calculation unit, with or without an "immediate load" instruction, the content of the M register 210 does not influence the actual loading of the AR register 230.

5 The bit positions are not reversed either in that case.

4) The multiplier element 58.

Multiplication is performed completely in parallel in accordance with the Booth's algorithm described in "A signed binary multiplier technique", by A.D. Booth, 10 Q.J. Mech. Appl. Math. 4 (1951), 236-240, and modified as published inter alia in "A proof of the modified Booth's algorithm for multiplication", by L.P. Rubinfeld, IEEE Trans. Computers (October 1976), pages 1014-1015. From two 16-bit operands on the outputs of the registers 50, 56 15 a 32-bit product word is formed in one machine cycle. The multiplier element is constructed so that the most significant bit is operative as having a negative value (sign bit). During the processing of operands in multiple precision the less significant parts thereof, therefore, do 20 not comprise a sign bit and the leading bit position must always be filled with a zero. This suppletion itself is described in the previous, non-published Netherlands Patent Application 8304186 (PHN 10 865) in the name of Applicant which is incorporated herein by way of reference.

25 To the output of the element 58 there are connected an accumulator adder 64 and an accumulator register 68, both elements having a width of 40 bits. If necessary, the sign bit in the register 60 (most significant bit of a product) is copied on more-significant 30 bits until a total number of 40 bits is reached. Furthermore two flag bits are provided in the program status register PST in the element 34 (alternatively, this number is increased)

a) when the permissible limits of the value range are exceeded, an overflow bit OVFL1 is made. The relevant 35 logic function is an EXCLUSIVE-OR function between the two most significant bits of the forty-bit accumulation/adding result.

PHN 10 886

17

31-8-1984
0154051

b) a second status bit SGNM indicates the sign of the accumulation result. The relevant logic function is an EXCLUSIVE-OR function between OVFL and the most significant bit but one of the accumulation/adding result.

If OVFL obtains the value "1" due to an arithmetic instruction, the bits OVFL, SGNM are fixed. They can then be modified only by program control, for example in that the content of the program status register in the arithmetic and logic unit is subjected to a modification operation. For as long as the bit OVFL retains the value "0", both status bits are interrogated after each arithmetic instruction used by the accumulator. The accumulation result is stored in the register 66 and applied to an element 62 for shift, extraction and reformatting operations. The output of the accumulator register 68 is fed back to the accumulator/adder 64.

5) Shift element 62.

Fig. 7 illustrates the shift element 62 in which reformatting operations are also performed. At the top of the Figure, the 40 bits arrive from the accumulator/adder 64. The sign extension operation is included in order to avoid an overflow condition as much as possible. This condition arises when the sum becomes too large due to addition of a number of successive numbers having the same sign. This risk is now reduced. On the input of the extractor 400 the most significant bit ACC39 is extended to fifteen more significant bit positions; this again is done for the detection of any overflow conditions. In the shift element 400 a 32-bit (double length) word is extracted from the 55 bits thus received. An operation can thus be performed with double the precision. At the left of the Figure there is shown a register (70) BSR which contains a four-bit code (bit 0...3). This code is decoded by the decoder 402. In this respect Fig. 7a shows the sixteen different extraction possibilities; the accumulator bits are supplemented by a least significant "0". Thus, the bits BSR 0 ... 3 with the codes 0000 ... 1111

PHN 10 886

18

3008154051

form sixteen staggered extracts of 32 bits each. The register 70 should be filled at least one instruction cycle before the actual extraction operation. The bits BSR 4, 5 are decoded by the decoder 404 which activates the reformatting device 406. The 32 extracted bits are referred to as E31 ... E0. The values of the bits BSR4, 5 control the following reformatting operation :

$\phi\phi$: the extraction 32-bit word is available to a user in the form of two half words;

1ϕ : the most significant bit of the least significant half word becomes " ϕ " and the remainder is shifted one position in the less-significant direction; the last bit of the extraction result is thus suppressed;

$\phi 1$: as $\phi\phi$, but the bits of the least significant half word are reversed. The elements 72, 72 are registers; the selection on the output thereof to the two buses is now denoted by separate selectors 73, 75 (not in Fig. 1). In addition to the 32 bits to be applied to the element 406, the extractor 400 also applies 9 more significant bits E31 ... E40 to the detector 408 which forms an overflow detector (and also receives bit E31). Should an inadmissible bit value (differing from E31) occur among these 9 bits, bit OOR in the program status register is set to "1"; this is because the relevant more significant bits must be repeats of the sign-indicating bit E31. The field MINS in the instruction which controls functions will be described in detail hereinafter.

6) The ALU unit 122.

Fig. 8 shows a block diagram of the arithmetic and logic unit 122 and its environment. The blocks 66, 118, 120, 122 are shown in Fig. 1. Block 119 represents a decoder for the field OPS for the instruction. Block 121 represents a decoder for the block AINS of the instruction. Block 125 represents a decoder for the relevant SX, SY, DX, DY fields of the instruction. To the output of the ALU element 122 there is connected a block 123 for the shift

PHN 10 886

19

30 8 1981
0154051

and rotation functions which will be described in detail hereinafter. The program status register PST is connected, using decoding elements not shown to the ALU 122 and the shift/rotation functions in the block 123.

- 5 The unit 122 operates in two's complement notation. Flag bits can be formed (a higher number would be feasible):
- Z : result of the ALU operation is "zero" ;
- N : result(interpreted as 2's-complement number) is negative;
- C : there is a carry signal, which may occur in unsigned
- 10 arithmetic operations for any less significant part of multiprecision words;
- O : overflow condition, which implies an error in the case of 2's complement notation. The bit "Z" is thus formed by detection of all bits of the operand together;
- 15 the bits C and N are formed by detection of a single bit, the overflow condition being detected in the same manner as described previously for the multiplier element.

The following operations are defined :

- 20 1. COM logic complement
2. AND logic AND-function
3. OR logic OR-function
4. EXOR logic EXCLUSIVE-OR function
5. ADD addition
- 25 6. XADD extended (multiprecision) addition; this means that during previous treatment of a less significant part of the operand any carry signal is stored for later treatment of a more significant part of the operand.
- 30 7. SUB subtraction
8. XSUB extended (i.e. multiprecision) subtraction; again a bit signal is carried between successively treated parts of an operand in given circumstances
9. NEG an arithmetical inversion
- 35 10. XNEG extended (multiprecision) inversion
11. CNEG conditional inversion
12. -
13. INC incrementation

PHN 10 886

20

30154051

- 14. XING extended(i.e. multiprecision) incrementation
- 15. DEC decrementation
- 16. XDEC extended (i.e. multiprecision) decrementation
- 17. NOP no action, flag bits retained
- 5 18. PASS conduct operand without modification
- 19. SWAP more significant and less significant bytes are
interchanged
- 20. CSUB conditional subtraction
- 21. -
- 10 22. ADDM add most significant bit of operand B to operand
A
- 23. XSGN copy N flagbit (indicating the sign) over 16 bits;
therefore, this is a "sign extension" as
described for the multiplier element.
- 15 24. ASL arithmetical shift to the left (more signifi-
cant direction)
- 25. XASL extended shift ditto
- 26. LSL logic shift to the left
- 27. LROL logic rotation to the left
- 20 28. ASR arithmetical shift to the right
- 29. XASR extended shift according to 28
- 30. LR logic shift to the right
- 31. LROR logic rotation clockwise
- 32. NULL generate output "0".

25 In the above list logic operations are performed
at the bit level. For arithmetical operations, the sign
bit or bits is (are) treated in a specific manner in given
circumstances. For the rotation operations, the shifted
out bit is added to the operand again at the opposite end.

30 For details of the sub-fields of the instruction,
reference is made to the Figures 13 (a-d). The connection
of the program status register PST (via a selector) to the
bus connection means is shown in simplified form.

Fig. 9 shows details of the structure of the

35 first accumulator means. It will be apparent that the
accumulator adder 122 is situated within the ALU. The memo-
ry MEM consists of a memory bank for 2^{n-1} words of $m = 16$

PHN 10 886

21

0154051
30.8.1984

bits each. It has a data input Y and two data outputs OUT1 and OUT2, each m bits wide. There are three separate address inputs ADRY, ADROUT1 and ADROUT2, each having a width of n bits (in this case $n = 4$). The first one is a write address, the other two being read addresses, each for the associated data connection. The three connections can be simultaneously and independently operative in one and the same instruction cycle.

7) Interrupt address register 24:

Register 24 is to be loaded from one of the buses and contains an address which is transferred to the program counter 30 at the beginning of an interrupt operation.

8) Program status register.

In this respect reference is made to Fig. 12 which shows the bit-wise subdivision of the sixteen-bit program status register (in element 34 in Fig. 1). The bits have the following meaning:

| | |
|-------|---|
| 0, 1 | : OVFL, and SGNM, the two bits disclosed with respect to the multiplier element and its environment |
| 2 | : OOR, overflow condition of the extractor |
| 3-6 | : Z, C, N, O, the four bits described with reference to the ALU unit, |
| 7-9 | : three flags reserved for the address calculation units |
| 10 | : IE interrupt admissible/not admissible |
| 11 | : FQR, instruction cycle selection bit; the last two bits can be modified by program control |
| 12-15 | : not used |

9) Input/ output status register (IOF).

This register forms part of the register bank 34 which comprises three registers. It contains status information and flag bits for communication with the environment. The bits have the following meaning: SIXACK denotes the degree of filling of the register 82 with valid information. SIYACK does so for the register

PHN 10 886

22

300154051

132. SOXACK indicates whether the register 84 is loaded with data. SOYACK serves the same purpose. PIACK : a transition from low to high on the \overline{WR} pin sets this flag bit to "1", synchronized by the separate clock (not shown) of the processor. When the data is read from the PI register (86), this flag is set to \emptyset again. POACK : a transition from low to high on the \overline{RD} pin sets this flag bit to "1", synchronized by the internal clock. When data is written in the P0 (86) register, this flag is set to \emptyset again. Two bits IFA, IFB in this register contain flag bits to be defined by a user; these flag bits may be interrogated via connection pins which are reserved on the integrated circuit for this purpose during the gesting of jump conditions.

10) Instruction repeat register 32.

This register 32 acts as a hardware instruction counter; when it is loaded with the value N, the next instruction is repeated N times. This register is decremented in reaction to the execution of | any | instruction, while the program counter in the element 30 can be incremented only when the content of register 32 is zero. Such repeating can be advantageously used notably for vector operations.

11) Description of the input/output structure.

The SOX (84) and SOY (132) connections can output data from the relevant data buses to the environment. To this end, each connection comprises a 16-bit register which can be synchronized by an external clock connection. These registers also receive internal request and enable signals as a synchronization handshake for a filling operation. Both outputs have a presettable counter for indicating the number of bits to be outputted.

The SIX (82) and SIY (130) connections can receive data from the environment for output to the relevant data buses. To this end, each connection comprises a serial input shift register which can be synchronized by an external clock connection. The input shift register

PHN 10 886

23

31-0154051

is connected in parallel to a buffer register for the feeding of the bus. Finally, these registers receive internal request and enable signals as a synchronization handshake for a read operation from the parallel register. There is
 5 also provided a presettable counter for controlling the number of bits to be loaded onto the buses in parallel.

The PI/PO (86) connection provides parallel transport to and from the processor, respectively. To this end, a 16-bit register is provided each time.

10 The additional output connection ADO(80) provides external transfer of data or addresses; the latter are calculated in an address calculation unit or in the arithmetic and logic unit. In this case there is provided a register which is to be selectively filled by both buses. These structures will be described in detail hereinafter with reference
 15 to some Figures. The set-up shown is substantially symmetrical with respect to the two buses. In other situations a less symmetrical set-up may be advantageous in order to save parts.
 12) Series connection status register (SIOST):

20 This is the last register of the register bank 34 which contains status information concerning the serial connections. The first four bits SILX3...0 of the 16 bits (actually the bit SILX 0 is the first bit of this status word) contain the word length for the series input shift register (of
 25 connection SIX); code 0000 means a word length of 16 bits and so on, so that finally the code 111 means a word length of 1 bit. The sequence bits SOLX3...0 the same for the connection SOX, the bits SILY3...0 the same for the connection SIY, and the bits SOLY3...0 the same for the connection SOY.

30 The interrupt mechanism:

External interrupt signals are represented by a low signal on the pin $\overline{\text{INT}}$ during at least 200 ns. This pin is interrogated every instruction cycle and so is the bit EI (enable bit) in the program status register. If EI = 1
 35 and $\overline{\text{INT}} = 0$, a branch operation is performed in the same cycle to the interrupt address (IAR register) and the bit IE is set to "0", the return address (content of program counter +1) being stored on the register stack. The

0154051

PHN 10 886

24

30.8.1984

switching over of the bit IE to "1" is performed under program control, after which in given circumstances the treatment of a next interrupt may commence. If subsequently $\overline{\text{INT}} = 1$ for an entire instruction cycle, all interrupt requests have been dealt with. Subsequently, the most recent return address is recalled from the stack registers.

Considering the size of the stack registers, 8 successive interrupt levels can be concurrently nested. The same is applicable to successive interrupt routines.

Finally there is provided a reset pin for resetting the ($\overline{\text{RST}}$) processor when this pin carries a low signal for at least 200 ns. The signal is stored in a flag flip-flop.

Parallel input/output structure:

Fig. 11a diagrammatically shows the input/output structure (parallel section). The buses 20/22, a 16-bit selector structure SEL, two parallel registers PI/PO, a tristate buffer TRISTBUFF, the external 16-bit bus D15 ... DO, a control unit PIOCONTR, and the control bits PIACK, POACK are shown. The signals $\overline{\text{RD}}$ and $\overline{\text{WR}}$ to be supplied by an external device have already been described. The bits PIRQ/PORQ are request bits to the environment.

Fig. 10 diagrammatically shows one of the two serial output connections. The output register (in this case SOX) is directly connected to the bus and feeds the output shift register SOXS. The presettable counter COD which can be loaded by the SIOST register is also shown. Output data may be taken up in SOXS only when this register is completely empty (determined by the counter content); in reaction thereto, SOXACK is set to "1" and new data may be applied; SOXRQ = 1 indicates a request to the environment and the counter is loaded. The output of the data to the environment commences when the pin SOXEN becomes "1", synchronization being performed by clock pulses on pin SOX. The tristate buffer TRIST is co-controlled by the value SOXEN. After the counter stops counting and no further data is waiting (SOACK = 1), bit SOXRQ is set to "0"

PHN 10 886

25

0154051
31-8-1984

so that SOXS and the counter assumes the "hold" state so that the last bit outputted remains on the pin DOX. When SOXEN becomes "0", the output circuit DOX assumes the high impedance initial state again.

5 Fig. 11 shows the serial input structure (in this case shown for the X-bus), comprising register SIX, input shift register SIXS, presetable counter COUN, and control and flag bit positions. When SIX is internally addressed as a data source, the flag SIXACK is set to "0" in the re-
10 gister IOF; it is valid for the next processor cycle. Data received in the shift register SIXS is transferred to the register SIX if the counter content indicates that the shift operation has been completed; the flag SIXACK then also becomes high in order to indicate the availability of
15 data to the processor. At the same time the flag bit SIXQR becomes high in order to inform the environment that the shift register SIXS may receive new data, the counter being loaded again with the length-indicating bits SILX3...SILX0; when this counter has been reset, the next data is com-
20 pletely present in the shift register SIXS. The serial input commences as soon as the input bit SIXEN becomes high after SIXQR has become high. Synchronization is provided by the serial clock CIX. When the counter has been completely reset and there is still data which has not been trans-
25 ferred to the register SIX, the flag bit SIXQR is set to "0" so that the counter and the shift register SIXS directly assume the "hold" mode.

Description of the fast mode of operation:

30 The operation of the processor has been described thus far for a 200 ns instruction cycle. When more use is made of a pipeline mechanism, the processor is also capable of implementing an instruction cycle of only 100 ns. In this respect reference is again made to Fig. 1; notably the registers 60 (at the output of the multiplier element), 46,
35 104, 88 (at the output of the data memory) also form part of the pipeline structure. By adaptation of the clock frequency the acceleration can be chosen so as to be less than a factor two.

Fig. 4 shows a time diagram for the operation.

PHN 10 886

26

3008154051

Therein, the bit FQR in the program status register PST continuously has the value "1".

In the "ALU" instruction, the following operations can be performed in parallel:

- 5 - an arithmetic/logic operation;
- at the most three address calculations for the memories;
- addressing of at the most three memory output registers;
- data transport on one or both buses.

10 In the "multiplication" instruction, the following operations can be performed in parallel:

- a multiplication operation;
- an accumulation/shift operation (elements 62, 64);
- at the most three address calculations for the memories;
- 15 - addressing of at the most three memory output registers;
- data transport on one or both buses.

In the "immediate load" instruction, the following operations can be performed in parallel:

- transporting data from the data field of the
- 20 instruction (in IR) to a destination on the X and/or Y bus;
- at the most three address calculations for the memories;
- addressing of at the most three memory output registers.

25 Line 300 in Fig. 4 indicates the successive cycles. On line 302 block 1 shows the address calculation. Block 1, line 304 represents the "read" access by way of the previously calculated address. The next block 2 indicates the time during which the data is valid in the

30 output register of the memory thus addressed. Block 1 of line 306 indicates that the transport takes place via the bus (buses) and possibly the processing in ALU and/or the multiplier element. Line 308 of block 2 (which is two blocks later than the block 1 on the line 306 in which

35 the processing is initiated) indicates that the processing result is valid in the output register of the multiplier element when addressed. On the other hand, an operation

PHN 10 886

27

0154051
308.1981

can similarly be performed in the ALU unit. Line 310 of block 1 indicates (in time before block 2 on line 308) that the address calculation for the next write operation (for the calculation result) may take place (in time
5 before block 2 on line 308). On line 312 block 1 indicates that a bus transport and possibly a write access in a memory take place.

The instruction register must now receive new data every 100 ns (so twice as fast as previously). The
10 register BSR must now also be filled one instruction cycle before the actual shift/reformatting operation and must remain valid for at least one instruction cycle. The flag bits EI (for the interrupt) and RESET (for resetting) are now interrogated every 100 ns.

15 A small difference with respect to the operations during the "slow" instruction cycle is that the output registers of the memories now act as source elements for the data bus (buses) instead of these memories themselves. Furthermore, all branch instructions and interrupt requests
20 must always be followed by an instruction which does not imply an operation (NOP); the content of the memories is thus saved.

Detailed description of the instruction set:

Referring to Fig. 2 again which shows the main
25 types of instruction words, some specific instruction fields will be described in detail hereinafter. Fig. 13a shows a table of the instruction field AINS of the arithmetic instructions. The first column gives the mnemonics. The second column shows the binary code. The last column
30 shows the operation on the flag bits Z, N, C, O. An asterisk in the first column means that only one operand is processed; consequently, this operand must arrive in the arithmetic and logic unit necessarily via the selector 66. A cross in the fourth column indicates that the filling
35 of the relevant flag bits is determined by the result of the operation. A "zero" (\emptyset) indicates that the relevant flag bit must be reset to zero. A horizontal dash indicates that the flag bit remains unmodified in all

PHN 10 886

28

0154051
30.8.1984

circumstances.

The field OPS selects the operands for the two inputs A (via register 120) and B (via register 118).

For the two-operand instructions, the bit C7 provides the control for the B input: "0" gates an operand from the bus 22; "1" gates the operand present in the register 118. Bit C8 provides the control for the A input: "0" gates the operand of the bus 20 and "1" admits the operand already present in the register 120. For the one-operand instructions (denoted by an asterisk in Fig. 13a), the register 118 is in the "hold" state, the codes 00, 01, 10 successively selecting the register 120, the bus 22 and the bus 20 in order to perform the operation on an associated operand. For the operation SWAP, the register 118 is in the hold mode; the code 01 selects the bus 22 and the code 10 selects the bus 20 for the operation; the register 120 is transparent.

Fig. 13b shows a table of the field MINS of the arithmetic instructions. There are seven code bits for 45 codes, so that a given degree of freedom of definition is obtained in order to facilitate the decoding. The codes can be divided into five groups, only the first group being shown in its entirety. The first column offers space for the code bits. The second column indicates the selection function for the elements 50/52. Thus, a transparency can be controlled (X) to the bus, or the content of the register can be used (MXL). Finally, a multiplier factor "-1" can be introduced. The third column indicates the selection function for the elements 54/56. A transparency (Y) can now be controlled to the bus, or the content of the register can be used (MYL); furthermore, the transparency can be controlled with an inversion. Always 200 ns is required for a multiplication operation. The fourth column shows the product thus formed.

The second group of codes is identical to the first group; moreover, the accumulator/adder 64 is activated in order to add the content of the register 68

PHN 10 886

29

0154051
30.8.1987.11

with a positive sign to the product of the two factors.
The third group is identical to the second group, except
that the content of the register 68 is now preceded by
a negative sign. The fourth group is identical to the
5 second group, except that the content of the register 68
is now shifted to the right through 15 bit locations (mul-
tiplication by 2^{-15}). The fifth group is identical to the
fourth group, except that the (shifted) content of the
register 68 is now preceded by a negative sign.

10 Fig. 13c shows two tables for the bus 20 and the
bus 22, respectively, in order to indicate that these
elements are capable of acting as a source for the bus.
Herein, ROM indicates element 90, ADO: element 80,
RAMA: element 36, ARB: element 106, RAMB: element 102,
15 IAR : element 24, SIX, SOC, PO, PI: the elements of the
input/output structure SIOST, PST, IOF: the registers of
the bank 34, BSR : element 70, MSP/LSP : elements 72/74,
R0 ... R14 : the registers of the bank 116, and PINR
the same as PI without treatment of pin PIQR. Finally
20 ARR is element 100, ARA element 48.

Fig. 13d shows two tables for the fields DX, DY.
Therein, the elements ACUA, ACUB, ACAR are the address
calculation units of the memories 36, 102, 90 respectively
The instruction field for this address calculation unit
25 determines which local register is loaded. For the element
116 the field R-file selects which of the registers is
loaded.

Finally the connection pins for signals will be
described.

30 CLK : clock for synchronizing internally derived
clock signals
RST : reset pin
D0...D15 : bidirectional I/O data pins
INT : pin for external interrupt
35 IFA, IFB : two flags to be defined by the user
A15...A0 : extra data outputs (parallel)
DIX, DIY : serial data inputs
DOX, DOY : serial data outputs

PHN 10 886

30

0154051
30.8.1984

SOXRQ, SOYRQ : serial input requests
 SOXEN, SOYEN : serial enable signals
 COX, COY : external asynchronous clock for serial
 data output
 5 SIXRQ, SIYRQ : request signals serial data input
 SIXEN, SIYEN : enable signals serial data input
 CIX, SIY : external asynchronous clock for serial
 data input
 \overline{RD} , \overline{WR} : read-write control for parallel I/O
 10 registers
 PORQ, PIRQ : request signals parallel input/output
 SYNC : output clock signals (in synchronism
 with instruction cycle) for synchronizing
 an external device.

15 Fig. 14 illustrates the multiplier element; the
 circuit arrangement will first be described. Corresponding
 elements are denoted by the same reference numerals as used
 in Fig. 1. Bus 20 is connected to the X-selector 54. Under
 the control of the bit SELX, the selector conducts either
 20 the bus operand or a value "-1" which is formed by a signal
 generator (not shown). Register 56 is made selectively
 transparent under control of bit ENX. The bus 22 is
 connected to the Y-selector 52. Under the control of the
 bit SELY, the selector gates either the bus operand
 25 or the arithmetically inverted value thereof. As a result
 of the two's complement notation used, this conversion
 is very simple. Register 50 is transparent or not under
 the control of the bit ENY. Thus, in the described manner
 three possibilities can be selected by the two control
 30 bits for each input of the multiplier element. The multi-
 plier element 58, moreover, receives a carry input signal:
 CARR. To the output of the multiplier element 58 there is
 connected a register PR. The accumulator/adder 64 does not
 receive special function signals. The accumulator register
 35 68 receives an enable signal ENA. Selector 69 is connected
 to the output of register 68 to allow the operand stored
 therein to be transferred, either without modification or

PHN 10 886

31

30 **0154051**

shifted over 15 bit positions in the less significant direction. The latter is again effected by the staggering of the connections. The selector 69 also receives an operand "0". Between the selector 69 and the accumulator/
5 adder 64 there is also included an inverter 71 which is selectively activatable by a signal PM.

The output of the accumulator/adder 64 is also connected to the shift element 62 which will not be described again herein. Figure 14a shows a control
10 table with six functions to be controlled for the element 64 in the first column. The right-hand columns of the Figure contain the required control signals. On line 1, the signals PM and SELA 1, 2 retain their previous value: the content of the register 68 then remains the same.

15

20

25

30

35

PHN 10 886

32

0154051
30.8.1984**CLAIMS**

1. A integrated and programmable processor for word-wise digital signal processing, comprising
- a. a multiplier element (58) which comprises a first input and a second input for receiving two operands for multiplication and a first output for presenting a product;
 - b. an arithmetic and logic unit (122) which comprises a third input and a fourth input for receiving two further operands, a second output for presenting a result operand and a first accumulator means (116) which are connected between the second output and the third input;
 - c. a first read-write memory (36, 102) for the storage of data;
 - d. connection means for connecting a control memory (28) for the storage of control information for the other components;
 - e. communication means, including bus connection means, for connecting said components to one another and to the environment,
- characterized in that
- f. said first input is connected to a separate first bus (22), said second input and fourth input being connected to a separate second bus (20) of said bus connection means;
 - g. said third input can be selectively coupled to the first bus;
 - h. said first accumulator means comprise a third output with a first selector means comprise a third output with a first selector for forming a selectable connection to said first and second bus;
 - i. said first output comprises a second selector (76) for forming a selectable connection to said first and second bus;

PHN 10 886

33

31-8-1984 **0154051**

j. said first read/write memory comprises an address input and a data input which are connected to said first and second bus, and a fourth output with a third selector (46, 104) in order to form a selectable connection to
5 said first and second bus.

2. An integrated processor as claimed in Claim 1, characterized in that said first read/write memory comprises a first memory module (36) whose address input is connected to the first bus and whose data input is connected to the second bus, and a second memory module (102)
10 whose address input is connected to the second bus and whose data input is connected to the first bus, the third selector comprising for each memory module a corresponding selection module (46, 104) which is connected to each of
15 the two buses, the connection for the control memory comprising an instruction register for storing control information for the control of further components, said instruction register (26) also having a data output connected to said bus connection means.

20 3. An integrated processor as claimed in Claim 2, characterized in that each of said first and second memory modules comprises its own address calculation unit (38, 114).

4. An integrated processor as claimed in Claim 1, 2
25 or 3, characterized in that said first output comprises retrocoupled second accumulator means, including accumulator adder means (64, 68), whereto there is connected a shift unit (62) for performing selectable shift and reformatting operations on data to be applied to the bus connection means.
30

5. An integrated processor as claimed in any one of the Claims 1 to 4, characterized in that said first accumulator means comprise a second read/write memory which is capable of storing several operands and which comprises
35 triple addressing means in order to allow for the simultaneous execution of a write operation from the arithmetic and logic unit to the second read/write memory as well as two independent read operations from the second read/write

PHN 10 886

34

0154051
30.8.1984

memory to the first bus and the second bus, respectively.

6. An integrated processor as claimed in any one of the Claims 1 to 5, characterized in that said control memory is also co-integrated.

5 7. An integrated processor as claimed in any one of the Claims 1 to 6, characterized in that there are provided further connection means for a further data memory (90) which is constructed as a read only memory and which
10 comprises an address connection to said bus connection means and a selectable data connection (88) to said first and second bus.

8. An integrated processor as claimed in Claim 7, characterized in that said further data memory comprises its own address calculation unit (92).

15 9. An integrated processor as claimed in Claim 7 or 8, characterized in that said further data memory is also co-integrated as a read-only memory.

10. An integrated processor as claimed in any one of the Claims 1 to 9, characterized in that said third
20 input comprises selector means for forming a selectable connection to said first and second bus.

11. An integrated processor as claimed in any one of the Claims 1 to 10, characterized in that there are provided timing means for controlling a first instruction
25 cycle which comprises the following coincident operations:

- address calculation for data memory, including associated memory access, in order to make an operand for the bus connection means available during the next instruction cycle;
- 30 - a data transport via at least one bus of the bus connection means;
- a data processing operation in at least one of the two elements arithmetic and logic unit and multiplier element on an operand transported via the bus connection means during said instruction cycle in order to
35 form a result operand during this instruction cycle, which operand is made available for transport via the

0154051

PHN 10 886

35

31-8-1984

bus connection means during the next or a subsequent instruction cycle.

12. An integrated processor as claimed in Claim 11, characterized in that there is provided a first cycle selector (FQR) which has a first state for controlling a first instruction cycle and a second state for controlling a second instruction cycle having a length which amounts to at least substantially half the length of the first instruction cycle, said second instruction cycle comprising the following coincident operations:

- address calculation for a data memory for the formation of an address for the next instruction cycle;
- memory access in a data memory by means of an address calculated during the directly preceding instruction cycle in order to make an operand available for the bus connection means in the next instruction cycle;
- a data transport via at least one bus of the bus connection means;
- a data processing operation in at least one of the two elements arithmetic and logic unit and multiplier element on at least one operand transported via the bus connection means during said instruction cycle or during a previous instruction cycle in order to form a result operand during the interval of the same instruction cycle plus the next instruction cycle in order to make this operand available for transport via the bus connection means during a second subsequent later instruction cycle, for which purpose output registers are connected to the multiplier element, and to the first read/write memory, said output registers being transparently activatable in said first state of the cycle selector, there being provided input registers for the arithmetic and logic unit and the multiplier element which are transparently activatable in both states of the cycle selector.

13. An integrated processor in which said first output comprises retrocoupled second accumulator means, including

PHN 10 886

36

31-8-1904 **0154051**

accumulator/adder means and a shift unit which is connected thereto, in order to perform selectable shift and reformatting operations on data to be applied to the bus connection means as claimed in any one of the Claims 1 to 12, characterized in that registers with selectively controllable input transparencies are connected between the inputs of the multiplier element and the bus connection means.

14. An integrated processor as claimed in Claim 13, characterized in that for at least one of the registers with selectively controllable input transparencies there are connected selector means for selectively performing an operand inversion or for gating a fixed quantity for supply to the multiplier element.

15. An integrated processor in which said first output comprises retrocoupled second accumulator means, including accumulator/adder means and a shift unit which is connected thereto, for performing selectable shift and reformatting operations on data to be applied to the bus connection means as claimed in any one of the Claims 1 to 14, characterized in that the retrocoupling is performed by means of an accumulator register in order to selectively present an accumulator result, inverted or not and/or shifted over a multiprecision bit shift interval, to the accumulator/adder means again.

16. An integrated processor as claimed in Claim 4, characterized in that the accumulator adder means accommodate sign extension bits as extension to the multiplication result.

17. An integrated processor as claimed in Claim 16, characterized in that the shift unit accommodates further extension bits in order to allow for a plurality of different extractions from the accumulation adder result available for the bus connection means under coded control.

18. An integrated processor as claimed in any one of the Claims 1 to 17, characterized in that for a data memory there is provided at least one address calculation unit

PHN 10 886

37

0154051
30.8.1984

which comprises an adder element for performing address accumulation which can be masked bit-wise under the control of a mask register.

19. An integrated processor as claimed in Claim
5 18, characterized in that the address calculation unit comprises a first register for an absolute address, a second register for a relative address, and a mask register, all said registers being connected to the bus connection means.

10

15

20

25

30

35

0154051

1/12

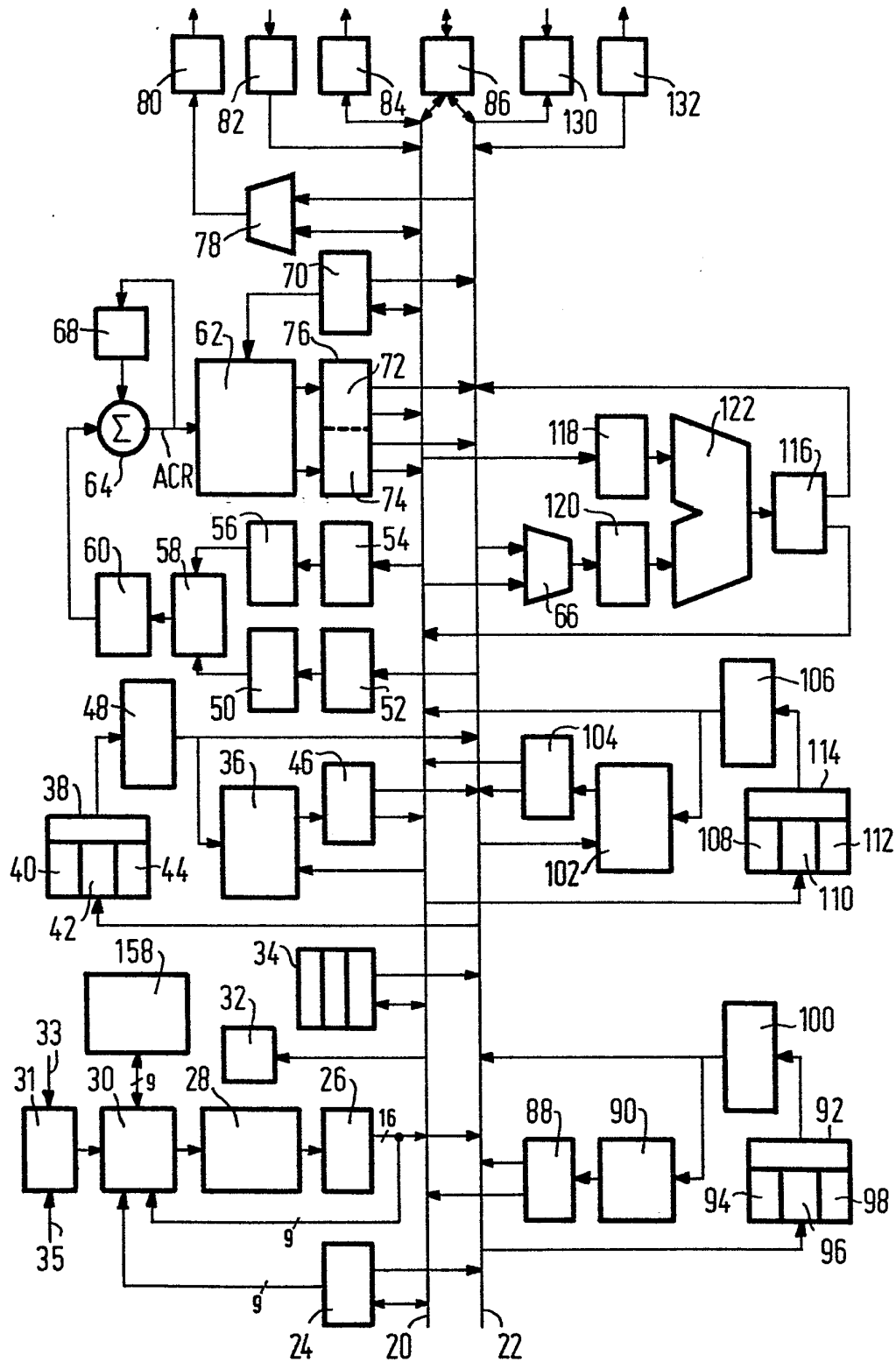


FIG. 1

0154051

2/12

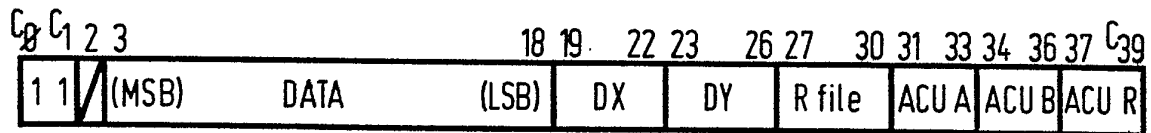
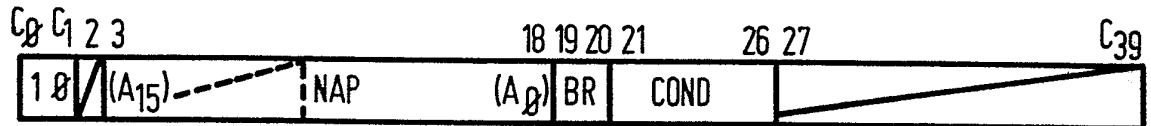
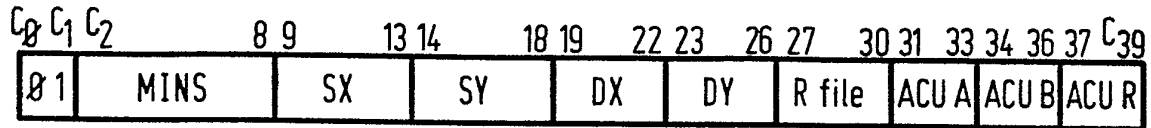
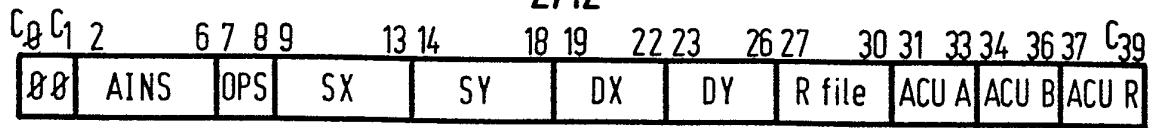


FIG.2

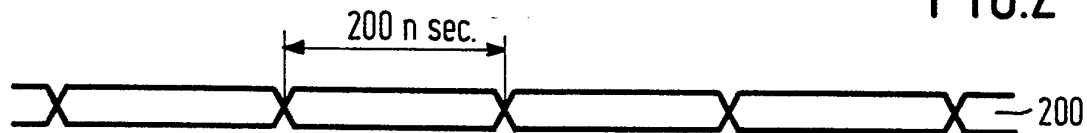


FIG.3



FIG.4



3/12

0154051

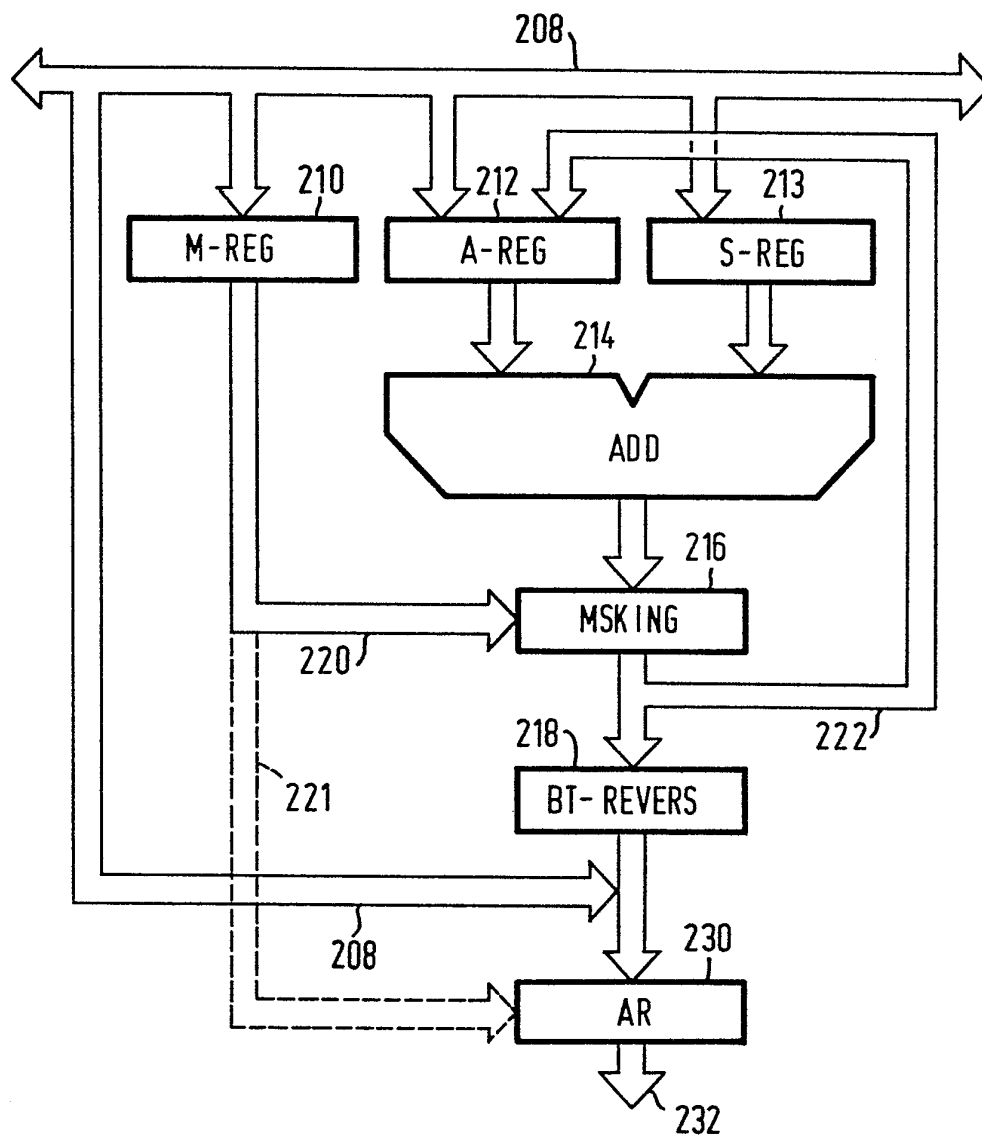


FIG. 5

4/12

0154051

| MNEM | C O D | O P E R A | | | |
|------|-------|---------------|-----------|-----------|------------------|
| | | AR_{new} | A_{new} | S_{new} | M_{new} |
| NOP | 0 0 0 | AR | A | S | M |
| INCA | 0 0 1 | $(A+1)mM$ | $(A+1)mM$ | S | M |
| DECA | 0 1 0 | $(A-1)mM$ | $(A-1)mM$ | S | M |
| STP | 0 1 1 | $(A+S)mM$ | $(A+S)mM$ | S | M |
| STM | 1 0 0 | $(A-S)mM$ | $(A-S)mM$ | S | M |
| FTCA | 1 0 1 | $(A)mM$ | $(A)mM$ | S | M |
| FTCS | 1 1 0 | $(S)mM$ | A | $(S)mM$ | M |
| BRAS | 1 1 1 | $BR((A+S)mM)$ | $(A+S)mM$ | S | M |
| LDIR | 0 0 0 | BUS | A | S | M |
| LDAA | 0 0 1 | BUS | BUS | S | M |
| LDAS | 0 1 0 | BUS | A | BUS | M |
| LDA | 0 1 1 | ADDR | BUS | S | M |
| LDS | 1 0 0 | ADDR | A | BUS | M |
| LDM | 1 0 1 | ADDR | A | S | BUS |
| LAAS | 1 1 0 | BUS | BUS | BUS | M |
| LALL | 1 1 1 | BUS | BUS | BUS | \overline{BUS} |

FIG.6

0154051

5/12

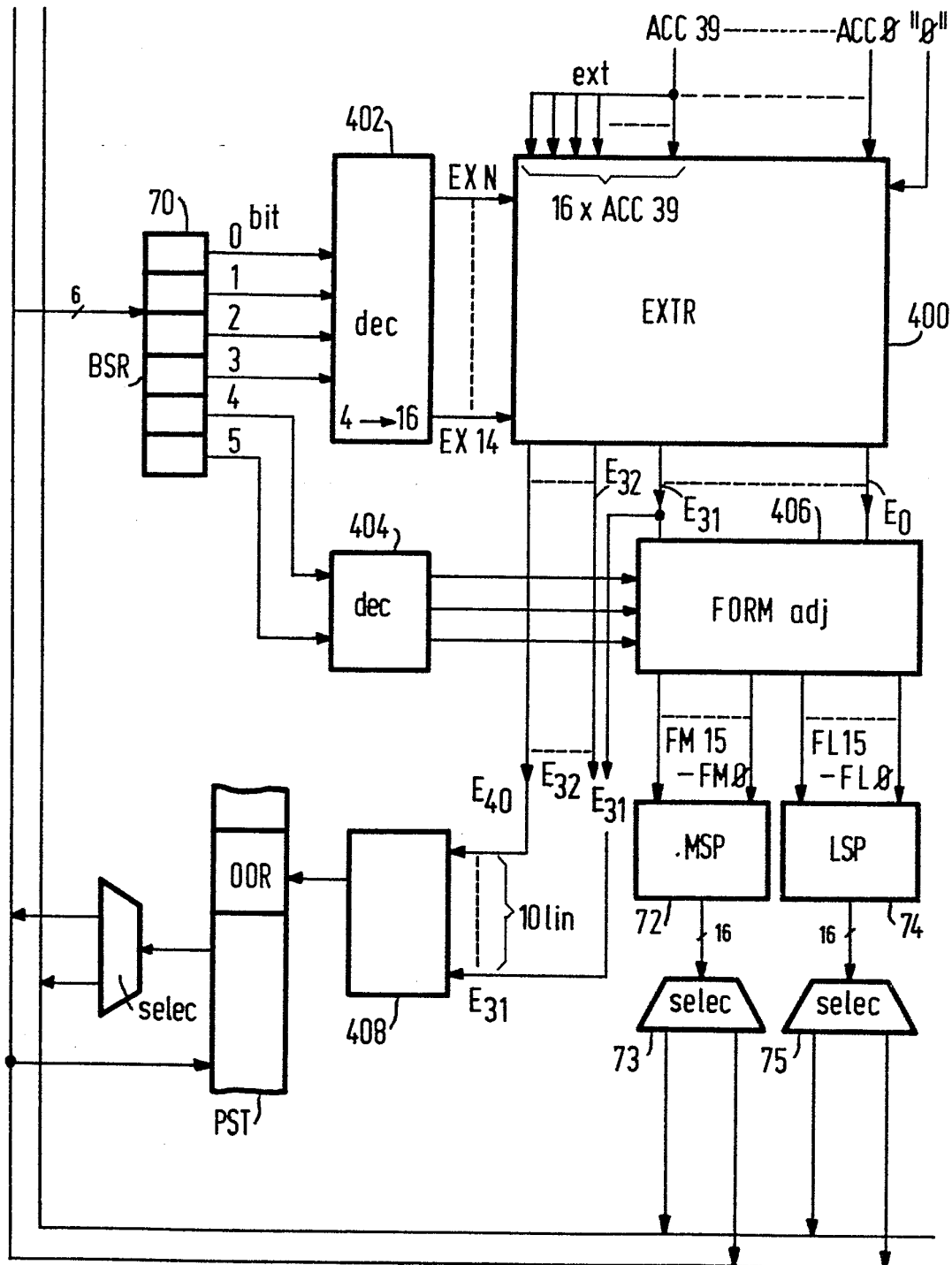


FIG. 7

0154051

6/12

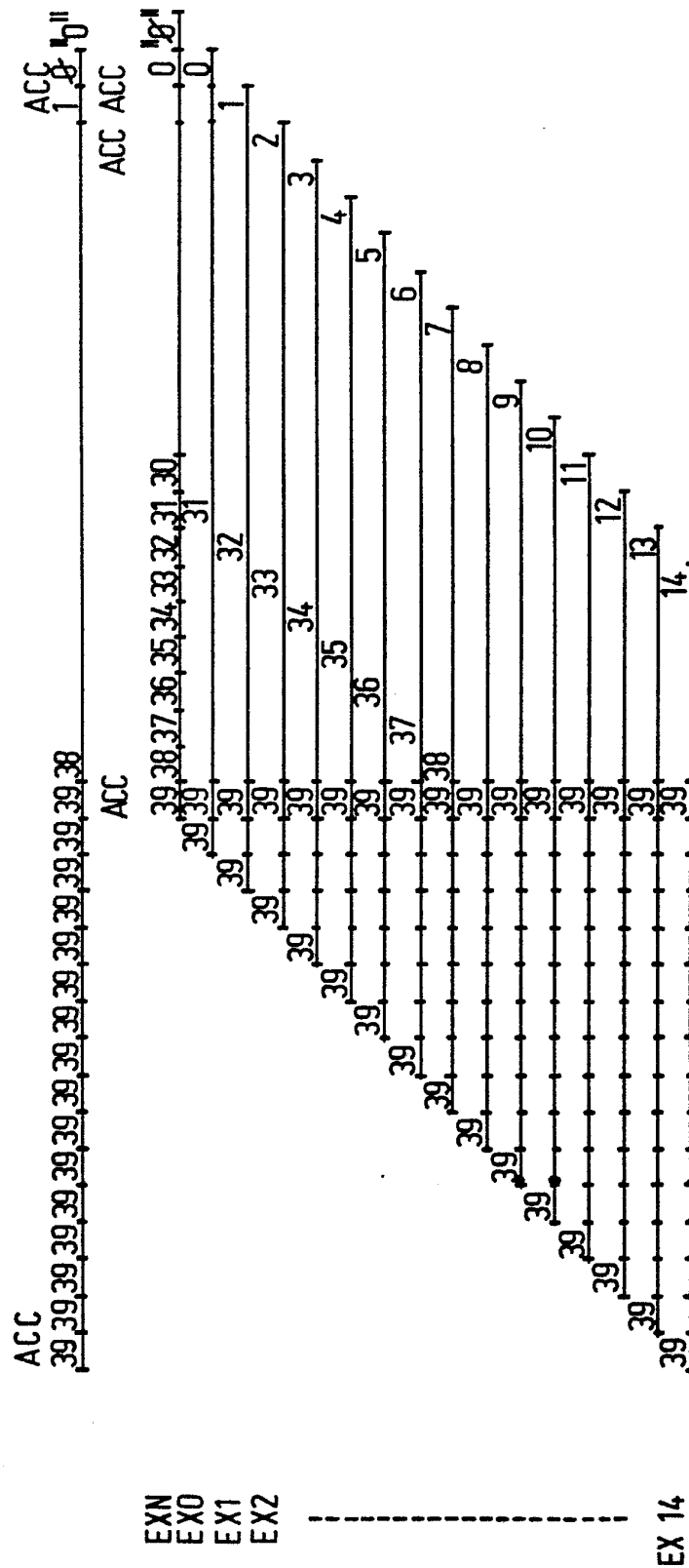
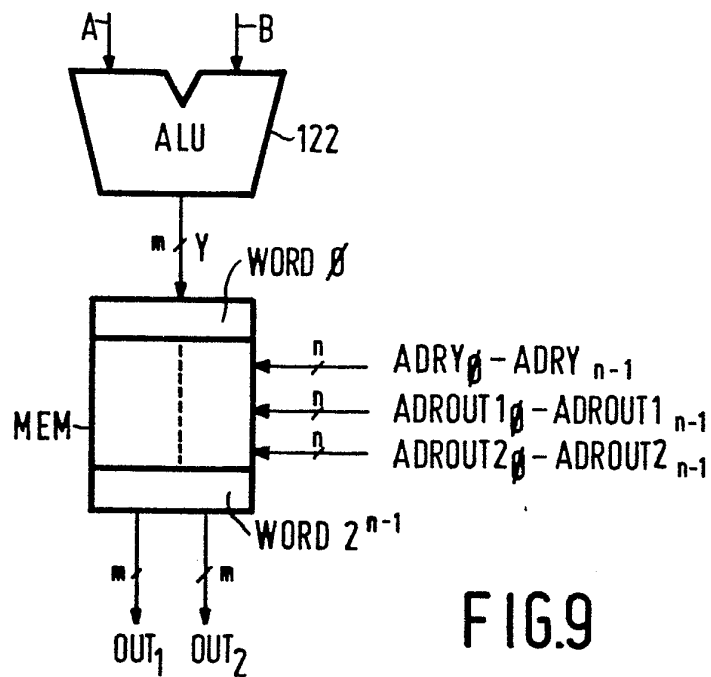
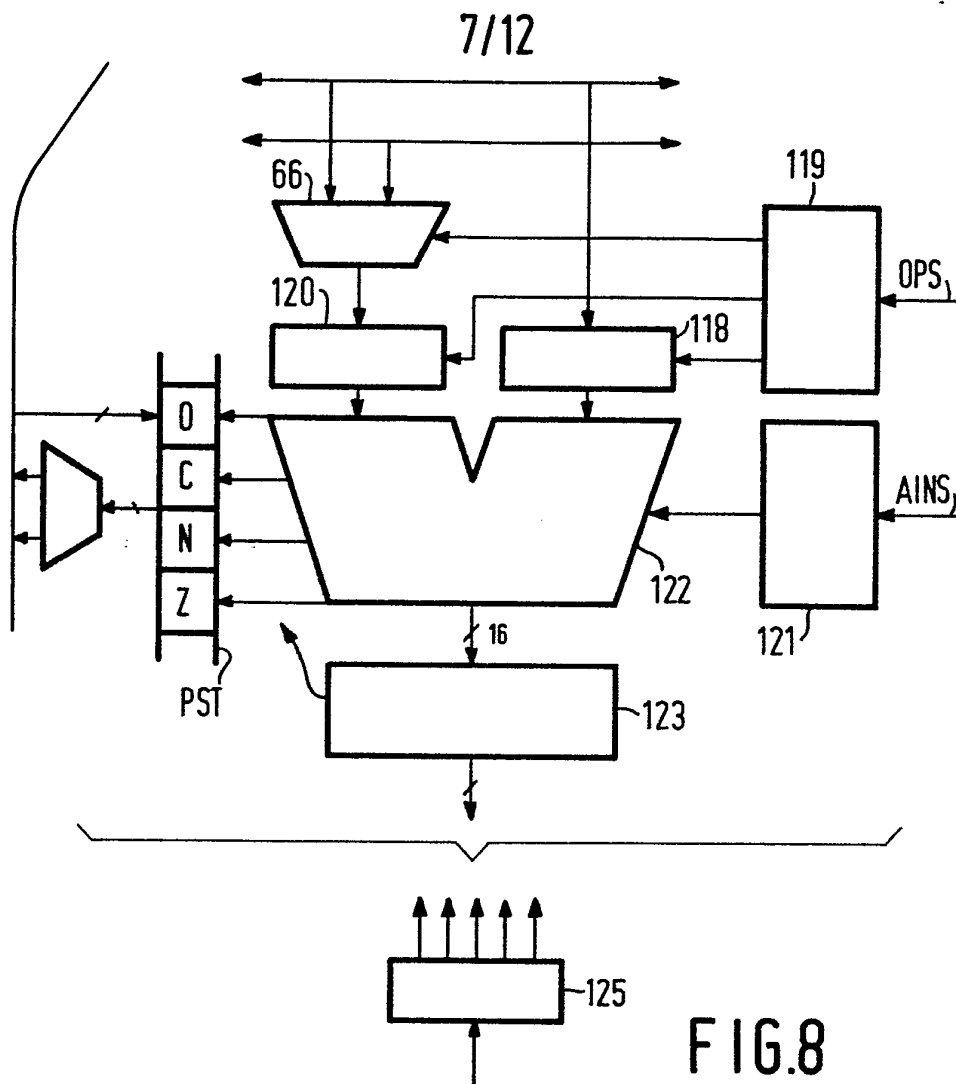


FIG. 7a

0154051



0154051

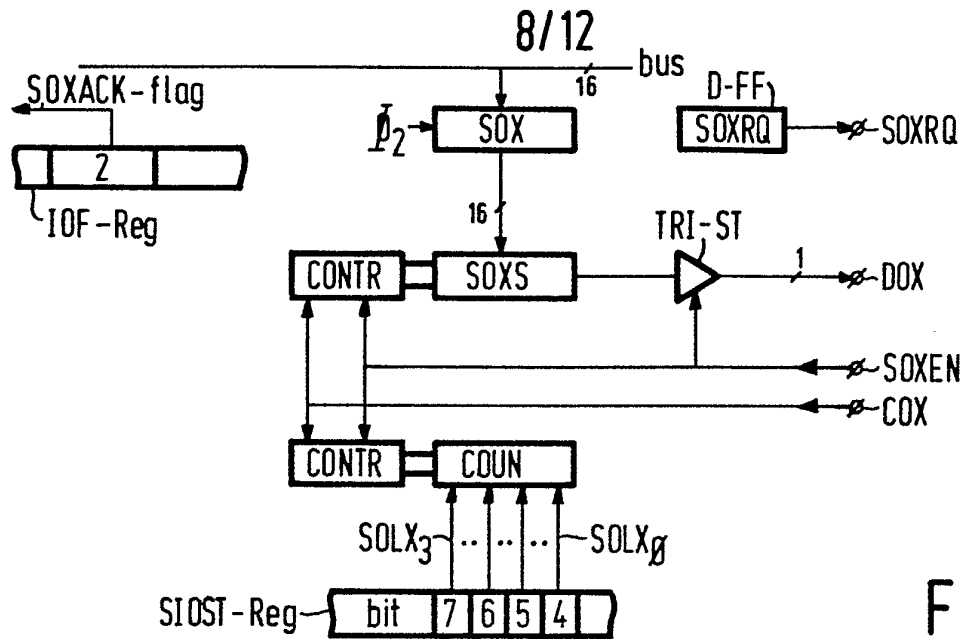


FIG. 10

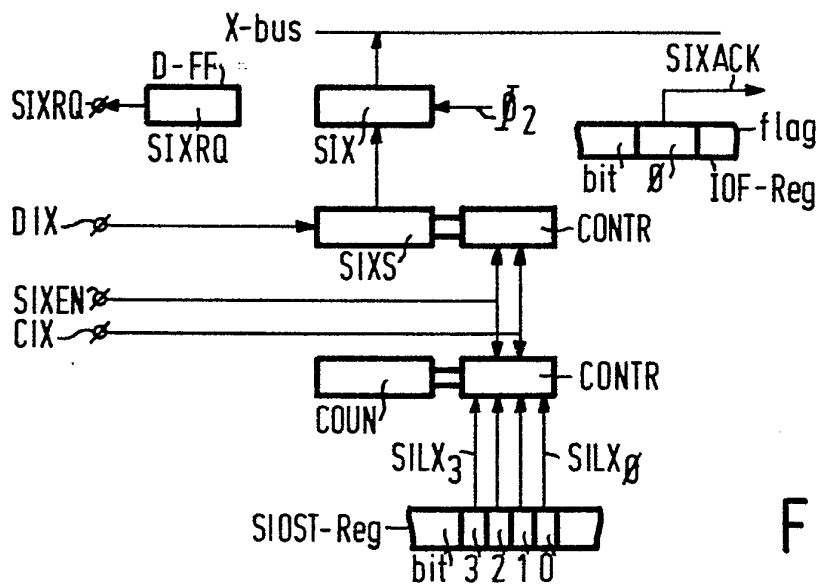


FIG. 11

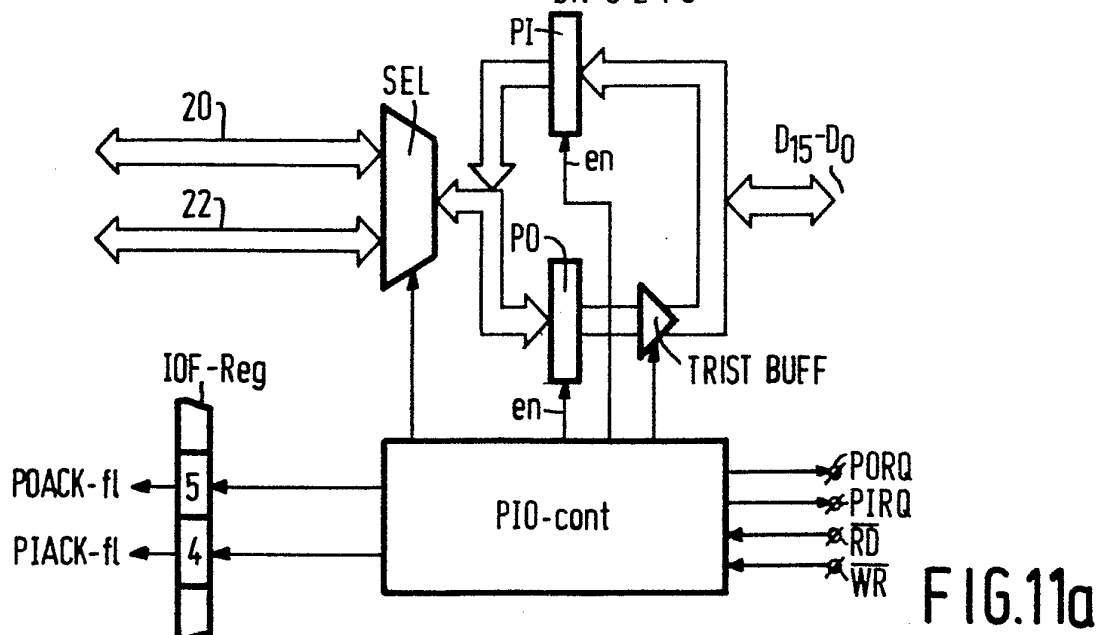


FIG. 11a

0154051

9/12

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|-----|---|---|---|---|-----|-----|-----|----|-----|----|----|----|----|
| | | 00R | Z | C | N | 0 | ACA | ACB | ACR | IE | FOR | - | - | - | - |

OVFL SGNM

FIG.12

| Mnem | AINS - Field | | | | | | Func | Flags Aff | | | |
|--------|----------------|---|---|---|----------------|--|------|-----------|---|---|---|
| | C ₂ | 3 | 4 | 5 | C ₆ | | | Z | N | C | O |
| COM* | 0 | 0 | 0 | 0 | 0 | | | x | x | 0 | 0 |
| AND | 0 | 0 | 0 | 0 | 1 | | | x | x | 0 | 0 |
| OR | 0 | 0 | 0 | 1 | 0 | | | x | x | 0 | 0 |
| EXOR | 0 | 0 | 0 | 1 | 1 | | | x | x | 0 | 0 |
| ADD | 0 | 1 | 0 | 0 | 0 | | | x | x | x | x |
| XADD | 0 | 1 | 0 | 0 | 1 | | | x | x | x | x |
| SUB | 0 | 0 | 1 | 1 | 0 | | | x | x | x | x |
| XSUB | 0 | 0 | 1 | 1 | 1 | | | x | x | x | x |
| NEG** | 0 | 1 | 1 | 0 | 0 | | | x | x | x | x |
| CNEG** | 0 | 1 | 1 | 0 | 1 | | | x | x | x | x |
| XNEG** | 0 | 1 | 1 | 1 | 0 | | | x | x | x | x |
| — | 0 | 1 | 1 | 1 | 1 | | | | | | |
| INC** | 1 | 0 | 1 | 0 | 0 | | | x | x | x | x |
| XINC** | 1 | 0 | 1 | 0 | 1 | | | x | x | x | x |
| DEC** | 1 | 0 | 1 | 1 | 0 | | | x | x | x | x |
| XDEC** | 1 | 0 | 1 | 1 | 1 | | | x | x | x | x |
| NOP** | 1 | 0 | 0 | 0 | 0 | | | - | - | - | - |
| PASS** | 1 | 0 | 0 | 0 | 1 | | | x | x | 0 | 0 |
| SWAP** | 1 | 0 | 0 | 1 | 0 | | | x | x | 0 | 0 |
| C SUB | 0 | 0 | 1 | 0 | 0 | | | x | x | x | x |
| — | 0 | 0 | 1 | 0 | 1 | | | | | | |
| ADDM* | 0 | 1 | 0 | 1 | 0 | | | x | x | x | x |
| XSGN* | 0 | 1 | 0 | 1 | 1 | | | x | - | x | 0 |
| NULL | 1 | 0 | 0 | 1 | 1 | | | x | x | 0 | 0 |
| ASL** | 1 | 1 | 0 | 0 | 0 | | | x | x | x | x |
| XASL** | 1 | 1 | 0 | 0 | 1 | | | x | x | x | x |
| LSL** | 1 | 1 | 0 | 1 | 0 | | | x | x | x | 0 |
| LROL** | 1 | 1 | 0 | 1 | 1 | | | x | x | x | 0 |
| ASR** | 1 | 1 | 1 | 0 | 0 | | | x | x | x | 0 |
| XASR** | 1 | 1 | 1 | 0 | 1 | | | x | - | x | 0 |
| LSR** | 1 | 1 | 1 | 1 | 0 | | | x | 0 | x | 0 |
| L ROR | 1 | 1 | 1 | 1 | 1 | | | x | x | x | 0 |

FIG.13a

10/12

0154051

| MINS | | | | | | | | Jnp Selec | | ACR= |
|----------------|----------------|---|---|---|---|---|---|-----------|-------|-------------|
| C ₂ | C ₃ | 4 | 5 | 6 | 7 | 8 | | P= | Q= | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | M X L | M Y L | A C R |
| | | | | | | | | X | Y | X·Y |
| | | | | | | | | X | -Y | -X·Y |
| | | | | | | | | M X L | Y | M X L·Y |
| | | | | | | | | M X L | -Y | -M X L·Y |
| | | | | | | | | X | M Y L | X·M Y L |
| | | | | | | | | M X L | M Y L | M X L·M Y L |
| | | | | | | | | -1 | -Y | Y |
| | | | | | | | | -1 | Y | Y |
| | | | | | | | | -1 | M Y L | -M Y L |

FIG.13b

| DX | | | | dest | | DY | | | | dest |
|-----------------|----|----|----|-------------|--|-----------------|----|----|-----------------|-------------|
| C ₁₉ | 20 | 21 | 22 | | | C ₂₃ | 24 | 25 | C ₂₆ | |
| 0 | 0 | 0 | 0 | n o n | | 0 | 0 | 0 | 0 | n o n |
| 0 | 0 | 0 | 1 | R A M A | | 0 | 0 | 0 | 1 | R A M B |
| 0 | 0 | 1 | 0 | A C U R * | | 0 | 0 | 1 | 0 | |
| 0 | 0 | 1 | 1 | A C U B * | | 0 | 0 | 1 | 1 | A C U A * |
| 0 | 1 | 0 | 0 | R P R * | | 0 | 1 | 0 | 0 | |
| 0 | 1 | 0 | 1 | I A R * | | 0 | 1 | 0 | 1 | |
| 0 | 1 | 1 | 0 | | | 0 | 1 | 1 | 0 | |
| 0 | 1 | 1 | 1 | S O X | | 0 | 1 | 1 | 1 | S O Y |
| 1 | 0 | 0 | 0 | P O | | 1 | 0 | 0 | 0 | P O |
| 1 | 0 | 0 | 1 | A D O | | 1 | 0 | 0 | 1 | A D O |
| 1 | 0 | 1 | 0 | S I O S T | | 1 | 0 | 1 | 0 | S I O S T |
| 1 | 0 | 1 | 1 | I O F | | 1 | 0 | 1 | 1 | I O F |
| 1 | 1 | 0 | 0 | P S T * | | 1 | 1 | 0 | 0 | |
| 1 | 1 | 0 | 1 | B S R * | | 1 | 1 | 0 | 1 | |
| 1 | 1 | 1 | 0 | | | 1 | 1 | 1 | 0 | |
| 1 | 1 | 1 | 1 | R F i l e ■ | | 1 | 1 | 1 | 1 | R F i l e ■ |

FIG.13d

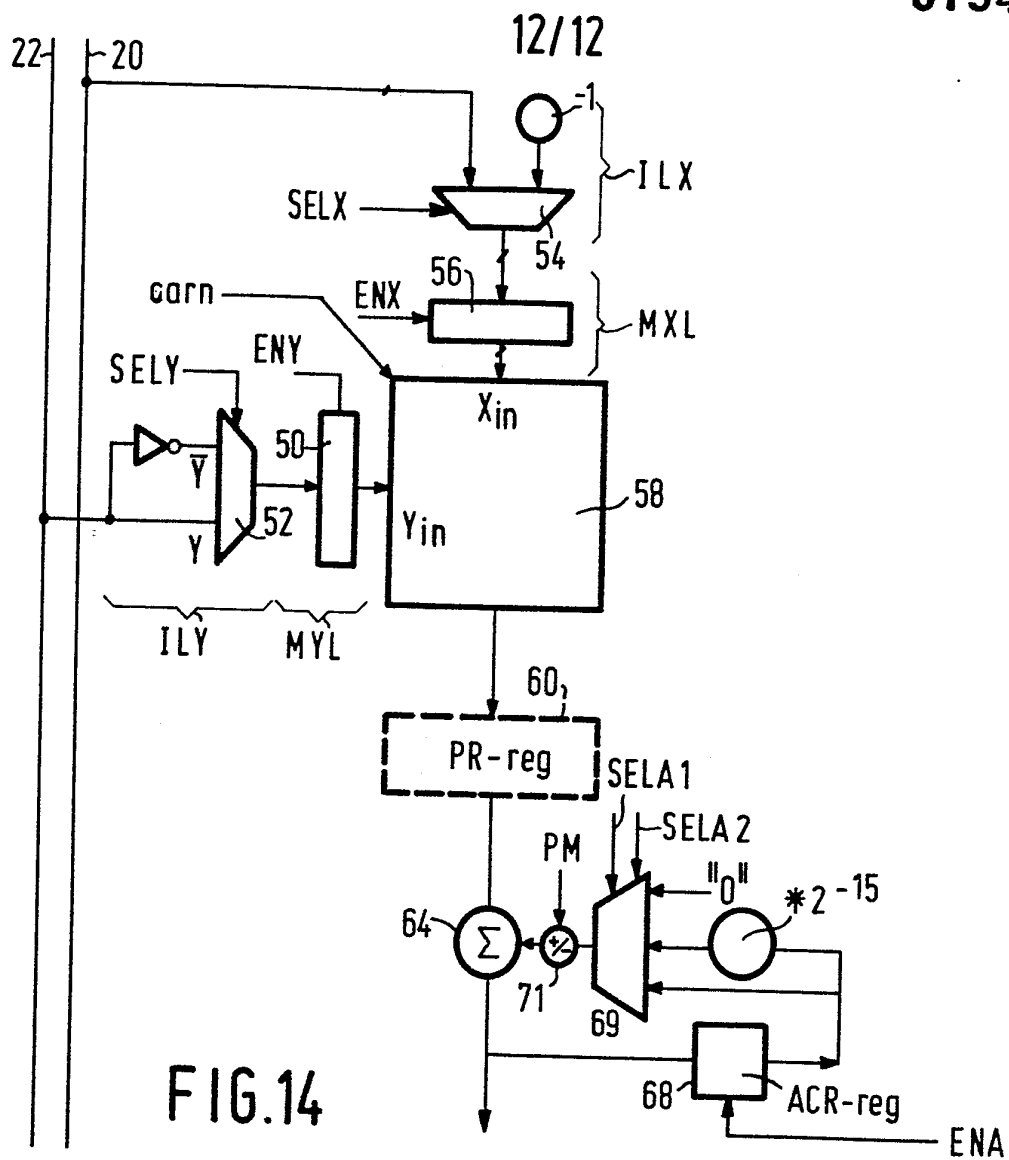
11/12

0154051

| S X C ₉ 10 11 12 C ₁₃ | | | | | Sel | S X C ₉ 10 11 12 C ₁₃ | | | | | Sel |
|---|---|---|---|---|-------|---|---|---|---|---|-----------|
| 0 | 0 | 0 | 0 | 0 | ROM | 1 | 0 | 0 | 0 | 0 | R 0 |
| 0 | 0 | 0 | 0 | 1 | ADD | 1 | 0 | 0 | 0 | 1 | R 1 |
| 0 | 0 | 0 | 1 | 0 | RAMA | 1 | 0 | 0 | 1 | 0 | R 2 |
| 0 | 0 | 0 | 1 | 1 | ARB | 1 | 0 | 0 | 1 | 1 | R 3 |
| 0 | 0 | 1 | 0 | 0 | RAMB | 1 | 0 | 1 | 0 | 0 | R 4 |
| 0 | 0 | 1 | 0 | 1 | IAR | 1 | 0 | 1 | 0 | 1 | R 5 |
| 0 | 0 | 1 | 1 | 0 | SIX | 1 | 0 | 1 | 1 | 0 | R 6 |
| 0 | 0 | 1 | 1 | 1 | SOX | 1 | 0 | 1 | 1 | 1 | R 7 |
| 0 | 1 | 0 | 0 | 0 | PO | 1 | 1 | 0 | 0 | 0 | R 8 |
| 0 | 1 | 0 | 0 | 1 | PI | 1 | 1 | 0 | 0 | 1 | R 9 |
| 0 | 1 | 0 | 1 | 0 | SIOST | 1 | 1 | 0 | 1 | 0 | R 10 |
| 0 | 1 | 0 | 1 | 1 | IOF | 1 | 1 | 0 | 1 | 1 | R 11 |
| 0 | 1 | 1 | 0 | 0 | PST | 1 | 1 | 1 | 0 | 0 | R 12 |
| 0 | 1 | 1 | 0 | 1 | BSR | 1 | 1 | 1 | 0 | 1 | R 13 |
| 0 | 1 | 1 | 1 | 0 | MSP | 1 | 1 | 1 | 1 | 0 | R 14 |
| 0 | 1 | 1 | 1 | 1 | LSP | 1 | 1 | 1 | 1 | 1 | P I N R * |
| | | | | | | | | | | | |
| S Y C ₁₄ 15 16 17 C ₁₈ | | | | | Sel | S Y C ₁₄ 15 16 17 C ₁₈ | | | | | Sel |
| 0 | 0 | 0 | 0 | 0 | ROM | 1 | 0 | 0 | 0 | 0 | R 0 |
| 0 | 0 | 0 | 0 | 1 | ARR | 1 | 0 | 0 | 0 | 1 | R 1 |
| 0 | 0 | 0 | 1 | 0 | RAMB | 1 | 0 | 0 | 1 | 0 | R 2 |
| 0 | 0 | 0 | 1 | 1 | ARA | 1 | 0 | 0 | 1 | 1 | R 3 |
| 0 | 0 | 1 | 0 | 0 | RAMA | 1 | 0 | 1 | 0 | 0 | R 4 |
| 0 | 0 | 1 | 0 | 1 | IAR | 1 | 0 | 1 | 0 | 1 | R 5 |
| 0 | 0 | 1 | 1 | 0 | SIY | 1 | 0 | 1 | 1 | 0 | R 6 |
| 0 | 0 | 1 | 1 | 1 | SOY | 1 | 0 | 1 | 1 | 1 | R 7 |
| 0 | 1 | 0 | 0 | 0 | PO | 1 | 1 | 0 | 0 | 0 | R 8 |
| 0 | 1 | 0 | 0 | 1 | PI | 1 | 1 | 0 | 0 | 1 | R 9 |
| 0 | 1 | 0 | 1 | 0 | SIOST | 1 | 1 | 0 | 1 | 0 | R 10 |
| 0 | 1 | 0 | 1 | 1 | IOF | 1 | 1 | 0 | 1 | 1 | R 11 |
| 0 | 1 | 1 | 0 | 0 | PST | 1 | 1 | 1 | 0 | 0 | R 12 |
| 0 | 1 | 1 | 0 | 1 | BSR | 1 | 1 | 1 | 0 | 1 | R 13 |
| 0 | 1 | 1 | 1 | 0 | MSP | 1 | 1 | 1 | 1 | 0 | R 14 |
| 0 | 1 | 1 | 1 | 1 | LSP | 1 | 1 | 1 | 1 | 1 | P I N R * |

FIG.13c

0154051



| Funct | PM | SELA 1 | SELA 2 | ENA |
|-----------------------|-------------------|----------------------|----------------------|-----|
| HOLD | PM _{old} | SELA1 _{old} | SELA2 _{old} | 0 |
| "0" | 1 | 0 | 0 | 1 |
| -ACR | 0 | 0 | 1 | 1 |
| +ACR | 1 | 0 | 1 | 1 |
| -ACR.2 ⁻¹⁵ | 0 | 1 | d.c | 1 |
| +ACR.2 ⁻¹⁵ | 1 | 1 | d.c | 1 |

FIG. 14a



European Patent
Office

EUROPEAN SEARCH REPORT

0154051

Application number

EP 84 20 1831

| DOCUMENTS CONSIDERED TO BE RELEVANT | | | |
|--|--|--|--|
| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl. 4) |
| Y | US-A-4 287 566 (G.J. CULLER) * Column 3, line 39 - column 4, line 33; column 9, line 19 - column 10, line 31 * | 1-4, 11 | G 06 F 9/38 G 06 F 7/48 |
| A | | 15, 18, 19 | |
| Y | --- PROCEEDINGS OF THE NATIONAL ELECTRONICS CONFERENCE, vol. 29, no. 29, October 1974, pages 416-421, New York, US; P.E. BLANKENSHIP et al.: "LSP/2 programmable signal processor" * Page 416, right-hand column, paragraph 2; page 418, left-hand column, paragraph 3 - page 420, paragraph 1 * | 1-4, 11 | |
| A | Idem | 16, 17 | |
| Y | --- PROCEEDINGS OF THE FALL 79 COMPCON-CONFERENCE, September 4-7, 1979, Pages 287-290, Washington, IEEE, New York, US; T. SAKAO et al.: "A single chip 4-bit microcomputer MN1500 series" * Page 287, right-hand column, last paragraph * | 1 | |
| | --- -/- | | |
| The present search report has been drawn up for all claims | | | |
| Place of search THE HAGUE | | Date of completion of the search 21-05-1985 | Examiner THOMAS K. |
| <p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</p> | | | |



European Patent
Office

EUROPEAN SEARCH REPORT

0154051

Application number

EP 84 20 1831

Page 2

| DOCUMENTS CONSIDERED TO BE RELEVANT | | | |
|--|---|--|--|
| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl. 4) |
| Y | EDN, vol. 25, no. 20, November 1980, Boston, US; "MCOM-42/43/44/45" * Page 119, figure * | 1 | |
| A | ICASSP82 PROCEEDINGS CONFERENCE, vol. 2, May 3-5, 1982, pages 1061-1064, Paris, IEEE, New York, US; D. KARLIN: "VLSI building blocks for digital signal processing" * Page 1064, left-hand column, paragraph 2 * | 1,5 | |
| A | GB-A-2 155 588 (SONY) * Page 2, line 43 - page 3, line 28 * | 1,5 | |
| A | US-A-4 075 704 (G.P. O'LEARY) | 1 | TECHNICAL FIELDS SEARCHED (Int. Cl. 4) |
| The present search report has been drawn up for all claims | | | |
| Place of search THE HAGUE | | Date of completion of the search 21-05-1985 | Examiner THOMAES K. |
| <p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</p> | | | |